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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/525,139	02/16/2005	Emmanuel Ardichvili	FR 020087	1770

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EXAMINER	
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ART UNIT	PAPER NUMBER
4142	

NOTIFICATION DATE	DELIVERY MODE
01/09/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/525,139	ARDICHVILI ET AL.	
	Examiner	Art Unit	
	Nay L. Htun	4142	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/16/2005, 5/19/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-13 are pending in this application.

2. Examiner acknowledges applicant's preliminary amendment filed on 2/16/2005; it is noted that claims 4-8, 10 have been amended.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d) based on French Patent Application No. ***0210452*** filed on ***8/21/2002***. The certified copy has been filed with US Application No. 10/525139, filed on ***02/16/2005***.

Drawings

4. The drawings filed on 02/16/2005 are acceptable for examination purpose.

Information Disclosure Statement

5. The information disclosure statements filed on 2/16/2005 and 5/19/2006 [1-15 pages] are in compliance with the provisions of 37 CFR 1.97 and have been considered and a copy is enclosed with this office action.

Specification

6. The abstract of the disclosure does not commence on a separate sheet in accordance with 37 CFR 1.52(b) (4). A new abstract of the disclosure is required and must be presented on a separate sheet, apart from any other text.

7. This application 10/525,139 is now US Pub No. 2006/0056542 A1. In the abstract, [line-2 **'sig al'**, line-3 **' nvention'**] should be **'signal'** and **'invention'**.

It appears that there are more than **'one'** typo error(s). Applicant is hereby required to review complete application to correct 'typo' or any other types of error(s).

8. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Also, the following appropriate Headings/titles, **bold** and **underlined**, are missing, applicant is hereby required to supply items (f, g, h, i, j).

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.
(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino

acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Claim Rejections - 35 USC § 112

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. **Claim 1, 12, 13 are rejected under 35 U.S.C. 112, second paragraph**, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

11. Regarding **claim 1**, it is unclear what is meant by "…**intended** to delay …" "…**intended** to write …" and "…**intended** to generate …" Moreover, "… **intended to** …" is indefinite as they lack concrete active limitation as to how the steps are to be accomplished. One of ordinary skill in the art would not be able to determine what exactly must be done to accomplish the goal of claim 1.

12. Regarding **claim 12**, it is unclear what is meant by "…**intended** to delay …" "…**intended** to write …" and "…**intended** to generate …" Moreover, "… **intended to** …" is indefinite as they lack concrete active limitation as to how the steps are to be accomplished. One of ordinary skill in the art would not be able to determine what exactly must be done to accomplish the goal of claim 12.

13. Regarding **claim 13**, it is unclear what is meant by "…**intended** to receive …" and "…**intended** to delay …" Moreover, "… **intended to** …" is indefinite as they lack concrete active limitation as to how the steps are to be accomplished. One of ordinary skill in the art would not be able to determine what exactly must be done to accomplish the goal of claim 13.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

16. **Claims 1-13 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Sourour et al., US Patent No. 6,363,105 B1 published on March 26, 2002 [hereafter Sourour] in view of Avital et al., US Patent No. 7,039,134 B1 filed on January 22, 2002 [hereafter Avital].**

17. Regarding **claim 1**, Sourour discloses 'A receiver (RECEP) for receiving an input signal comprising a series of samples (IN_TIME, EARLY, LATE, VOID)' [see abstract], series of samples corresponds to Sourour's group of samples. 'said receiver (RECEP) comprising one

delay line (D_LINE) [fig 8A, element 804; col 5, line 13], characterized in that the delay line (D_LINE) is intended to delay said input signal by a series of delays (τ) and is divided into a series of delay sub-lines (ZONE) [fig 8A, element 606, col 5, line 14] each intended to write one from the series of samples (IN_TIME, EARLY, LATE, VOID) of said input signal (INPUT)' [fig 8A, element 804, 802; col 5, line 15-16], delay sub-lines corresponds to Sourour's multiple delay taps.

It is noted that Sourour does not explicitly teach 'in that the solution comprises control means (RD_ADD_GEN) intended to generate read addresses of the samples in the delay sub-lines (ZONE) from the series of samples (IN_TIME, EARLY, LATE, VOID) of the input signal (INPUT), so that a read address is equal to a difference between a write address of a sample in a delay sub-line (ZONE) of the input signal and a delay (τ) expressed as a number of sampling periods from the series of delays (τ).'

On the other hand, Avital teaches 'in that the solution comprises control means (RD_ADD_GEN) intended to generate read addresses of the samples in the delay sub-lines (ZONE) from the series of samples (IN_TIME, EARLY, LATE, VOID) of the input signal (INPUT)' [fig 8, col 14, line 49-52], control means corresponds to Avital's correlator. 'so that a read address is equal to a difference between a write address of a sample in a delay sub-line (ZONE) of the input signal and a delay (τ) expressed as a number of sampling periods from the series of delays (τ)' [col 14, line 57-61].

It would have been obvious to the one skilled in the art at the time of applicant's invention was made to incorporate storing and outputting input signals parallel to the shift registers in reduced complexity correlators taught by Avital into input signal received by delay

lines with multiple delay taps in flexible sliding correlators taught by Sourour because both Avital and Sourour are directed to spread spectrum receiver with correlators having less power consumption and reduced number of gates on chip [Sourour: col-4, line 14-15; Avital: col-3, line 29-32].

It would have been obvious to the one skilled in the art at the time of applicant's invention was made to incorporate storing and outputting input signals parallel to the shift registers in reduced complexity correlators taught by Avital into input signal received by delay lines with multiple delay taps in flexible sliding correlators taught by Sourour because that would have allowed users of Sourour to use multi path signals with different delay times capable of performing correlation of delays of input signals or sampling streams as detailed in Avital [col-4, line 20-40], thereby bringing the advantages of quality and reliability of fast sampling in digital and pulse communication.

Therefore it would have been obvious to the person skilled in the art at the time of invention was made to implement generating and grouping input signals with corresponding code sequences and samplings taught by Sourour with Avital's method of storing and outputting received signals, thereby predicting sampling result with specific delay(s).

18. Regarding **claim 2**, Sourour discloses 'the delay line comprises a single series of delay sub-lines' [fig 8, element 800, 804; col 5, line 13-14].

19. Regarding **claim 3**, Sourour discloses 'the delay line comprises various series (BANK) of delay sub-lines' [fig 8, element 800, 804; col 5, line 13-15].

20. Regarding **claim 4**, Sourour discloses 'a delay sub-line (ZONE) is accessible with a frequency twice as fast as the samples of an input signal received by the receiver (RECEP)' [col 7, line 7-13].

21. Regarding **claim 5**, Avital discloses 'one memory area is associated to one delay sub-line (ZONE)' [fig 4, element 100, 104; col 11, line 44-47].

22. Regarding **claim 6**, Avital discloses 'the samples of a series of samples (IN_TIME, EARLY, LATE, VOID) are accessible in parallel in the write mode or read mode in the delay sub-lines (ZONE)' [fig 4, element 102; col 11, line 47-50].

23. Regarding **claim 7**, Avital discloses 'the read addresses of the samples of a series of samples (IN_TIME, EARLY, LATE, VOID) are situated at addresses immediately adjacent or equal to one another' [fig 4; col 11, line 57-60].

24. Regarding **claim 8**, Sourour discloses 'two series of samples (C_CHIP, NEXT_CHIP) are read in parallel' [col 7, line 66-67, col 8, line 1].

25. Regarding **claim 9**, Sourour discloses 'the delay line (D_LINE) comprises selection means (SELECT_BANK) of a series (BANK) of delay sub-lines to which belongs one of the two series of samples read as a function of the delay (τ)' [fig 8B, element 852, 812; col 8, line 3-9].

26. Regarding **claim 10**, Avital discloses 'the delay line (D_LINE) comprises a position factor (DOWN_POS) indicating the position of a reference sample (IN_TIME) from a series of samples (IN_TIME, EARLY, LATE, VOID) of an input signal in the series of delay sub-lines to which it belongs' [col 14, line 37-41].

27. Regarding **claim 11**, Sourour discloses 'the memory areas (ZONE) are regrouped into a first and a second group (GROUPEA, GROUPEB), the first group regrouping a current series of current areas (C_BANK) and a next series of areas (NEXT_BANK) which can each correspond to the first series (BANK0) of delay sub-lines and the second group regrouping a current series of areas (C_BANK) and a next series of areas (NEXT_BANK) which can each correspond to the second series (BANK1) of the delay sub-lines, so that the memory areas for a series of samples read are identical for each equal position factor value (DOWN_POS)' [fig 8A, element 608, 809, 811; col 10, line 50-57].

Regarding **claim 12**, Sourour discloses 'A delay line (D_LINE) for delaying an input signal (INPUT), said input signal comprising a series of samples, (IN_TIME, EARLY, LATE, VOID), [abstract; fig 8A, element 804; col 5, line 13], series of samples corresponds to Sourour's group of samples. 'characterized in that the delay line is intended to delay said input signal by a series of delays (τ) and is divided into a series of delay sub-lines (ZONE) each intended to write one from the series of samples (IN_TIME, EARLY, LATE, VOID) of said input signal (INPUT),' [fig 8A, element 804, 802; col 5, line 15-16], delay sub-line corresponds to Sourour's multiple delay taps.

It is noted that Sourour does not explicitly teach 'in that the delay line comprises control means (RD_ADD_GEN) intended to generate read addresses of the samples in the delay sub-lines (ZONE) from the series of samples (IN_TIME, EARLY, LATE, VOID) of the input signal (INPUT), so that a read address is equal to a difference between a write address of a sample in a

delay sub-line (ZONE) of the input signal and a delay (τ) expressed as a number of sampling periods from the series of delays (τ)'.

On the other hand, Avital teaches 'in that the delay line comprises control means (RD_ADD_GEN) intended to generate read addresses of the samples in the delay sub-lines (ZONE) from the series of samples (IN_TIME, EARLY, LATE, VOID) of the input signal (INPUT)' [fig 8, col 14, line 49-52], control means corresponds to Avital's correlator. 'so that a read address is equal to a difference between a write address of a sample in a delay sub-line (ZONE) of the input signal and a delay (τ) expressed as a number of sampling periods from the series of delays (τ)' [col 14, line 57-61].

It would have been obvious to the one skilled in the art at the time of applicant's invention was made to incorporate storing and outputting input signals parallel to the shift registers in reduced complexity correlators taught by Avital into input signal received by delay lines with multiple delay taps in flexible sliding correlators taught by Sourour because both Avital and Sourour are directed to spread spectrum receiver with correlators having less power consumption and reduced number of gates on chip [Sourour: col-4, line 14-15; Avital: col-3, line 29-32].

It would have been obvious to the one skilled in the art at the time of applicant's invention was made to incorporate storing and outputting input signals parallel to the shift registers in reduced complexity correlators taught by Avital into input signal received by delay lines with multiple delay taps in flexible sliding correlators taught by Sourour because that would have allowed users of Sourour to use multi path signals with different delay times capable of performing correlation of delays of input signals or sampling streams as detailed in Avital [col-4,

line 20-40], thereby bringing the advantages of quality and reliability of fast sampling in digital and pulse communication.

Therefore it would have been obvious to the person skilled in the art at the time of invention was made to implement generating and grouping input signals with corresponding code sequences and samplings taught by Sourour with Avital's method of storing and outputting received signals, thereby predicting sampling result with specific delay(s).

28. Regarding **claim 13**, Sourour discloses 'A method of delaying an input signal (INPUT) by means of a delay line (D_LINE), said input signal comprising a series of samples (IN_TIME, EARLY, LATE)', [fig 8A, element 804; col 5, line 13], series of samples corresponds to Sourour's group of samples.

'characterized in that it comprises the steps of:'

'dividing the delay line (D_LINE) into a series of delay sub-lines (ZONE) each intended to receive a sample from the series of samples (IN_TIME, EARLY, LATE, VOID) of the input signal (INPUT), series of samples corresponds to Sourour's group of samples. 'said delay line being intended to delay said input signal by a series of delays (τ) and' [fig 8A, element 804, 802; col 5, line 15-16].

It is noted that Sourour does not explicitly teach 'generating read addresses of the samples in the delay sub-lines (ZONE) from the series of samples of the input signal (INPUT), so that a read address is equal to a difference between a write address of a sample in a delay sub-

line (ZONE) of the input signal and a delay (τ) expressed as a number of sampling periods of the series of delays (τ).'

On the other hand, Avital teaches 'generating read addresses of the samples in the delay sub-lines (ZONE) from the series of samples of the input signal (INPUT), [fig 8, col 14, line 49-52], so that a read address is equal to a difference between a write address of a sample in a delay sub-line (ZONE) of the input signal and a delay (τ) expressed as a number of sampling periods of the series of delays (τ)' [col 14, line 57-61].

It would have been obvious to the one skilled in the art at the time of applicant's invention was made to incorporate storing and outputting input signals parallel to the shift registers in reduced complexity correlators taught by Avital into input signal received by delay lines with multiple delay taps in flexible sliding correlators taught by Sourour because both Avital and Sourour are directed to spread spectrum receiver with correlators having less power consumption and reduced number of gates on chip [Sourour: col-4, line 14-15; Avital: col-3, line 29-32].

It would have been obvious to the one skilled in the art at the time of applicant's invention was made to incorporate storing and outputting input signals parallel to the shift registers in reduced complexity correlators taught by Avital into input signal received by delay lines with multiple delay taps in flexible sliding correlators taught by Sourour because that would have allowed users of Sourour to use multi path signals with different delay times capable of performing correlation of delays of input signals or sampling streams as detailed in Avital [col-4,

line 20-40], thereby bringing the advantages of quality and reliability of fast sampling in digital and pulse communication.

Therefore it would have been obvious to the person skilled in the art at the time of invention was made to implement generating and grouping input signals with corresponding code sequences and samplings taught by Sourour with Avital's method of storing and outputting received signals, thereby predicting sampling result with specific delay(s).

Conclusion

Prior art made of record.

a. US Patent No. 6,363,105 B1

b. US Patent No. 7,039,134 B1

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

c. US Patent No. 6,480,527 B1

d. US Patent No. 6,560,273 B1

e. US Patent No. 6,967,939 B2

f. US Patent No. 7,039,134 B1

g. US Pub. No. 2003/0235238 A1

h. US Pub. No. 2006/0056542 A1

i. US Pub. No. 2003/0231705 A1

j. W. Namgoong et al., "Power Consumption of Parallel Spread Spectrum Correlator Architectures", Low Power Electronics and Design, 1998. Proceedings, 1998 International Symposium on 10-12 Aug.1998 pp: 133-135.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NAY L. HTUN whose telephone number is (571)270-3914. The examiner can normally be reached on Monday - Thursday from 8:00 a.m. to 6:00 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Srirama Channavajjala, can be reached on (571) 272-4108. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NH

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